Deliberate Practice

Variation-Resilient Building Blocks for Ultra-Low-Energy Sub-Threshold Design

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Robust
Low
Power
VLSI

Motivation

- Energy minimization for BSNs
- Operate circuits in sub-threshold
- Tradeoffs
  - Sensitivity to variation
  - Performance

Metrics for Evaluation

1. Energy Consumption
2. Gate Delay
3. Delay Variation $\left(\frac{\sigma}{\mu}\right)$
4. Robustness
    1. $\frac{I_{on}}{I_{off}}$
    2. Noise Margins (output swing)
5. Area overhead

Attacking the Problem

Block/Logic Level

- ???

Standard Cells

- ???

Device Level

- ???

Research Questions

1. How do you design sub-threshold standard cells capable of MHz operation that are variation-resilient?

Answers from Week 2

1. Use technologies meant for sub-threshold (MITLL)
2. Use minimum sized standard cells to trade off energy and performance
3. Use different logic families (e.g. NAND only or not CMOS)
4. Custom standard cell library (PyCell?)
5. Use redundancy in logic paths (like RAZOR). Have a reliability vs. area tradeoff.
6. Increase the length of the transistors. Hurts performance but reduces energy.

Paper's Solutions

1. Focus on **standard cells**
    1. Low-Vt transistors
        1. Improved performance

Research Questions

2. For an inverter, what design choices can we do to make it variation resilient?
   - Area overhead
   - Delay Variation $\left(\frac{\sigma}{\mu}\right)$
   - Robustness
     - $\frac{I_{on}}{I_{off}}$
     - Noise Margins (output swing)

Answers from Week 2

1. Adjust sizing to balance the P to N ratio
2. Mixed Vt inverter
3. Schmitt trigger inverter
4. Mixed-length NMOS

Paper's Solutions

1. Focus on **standard cells**
    1. NMOS Stacking in gates
        1. Can relax PMOS sizing
        2. Decreases the delay variation
    2. Balance N/PMOS strengths to maximize noise margin
        1. Get rid of sizing with transmission gate logic

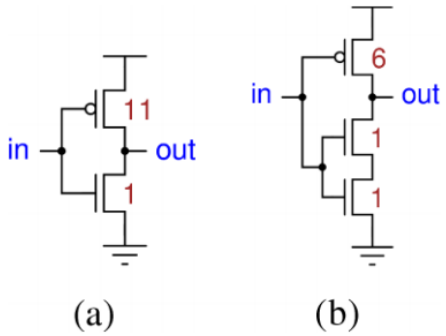
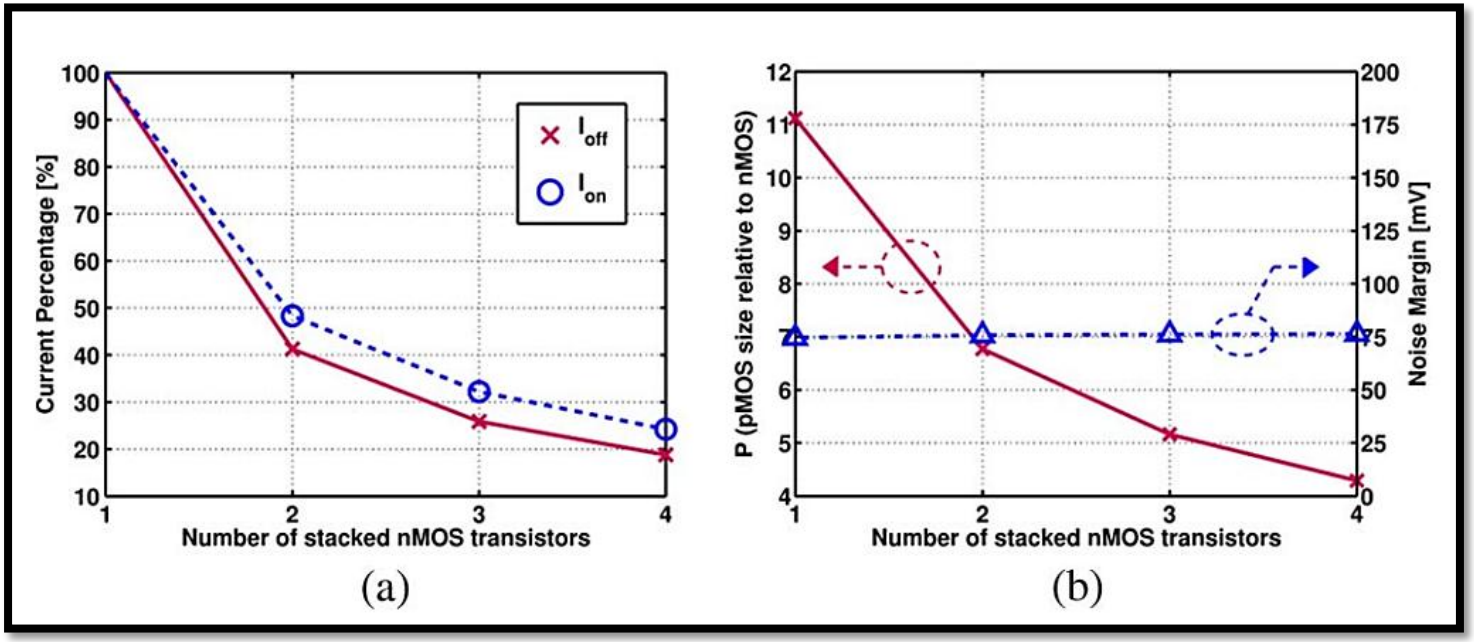


Fig. 2. Schematic of (a) a standard CMOS inverter sized for sub-threshold operation and (b) a stacked nMOS inverter with relaxed pMOS sizing.

NMOS Stacking



Research Questions

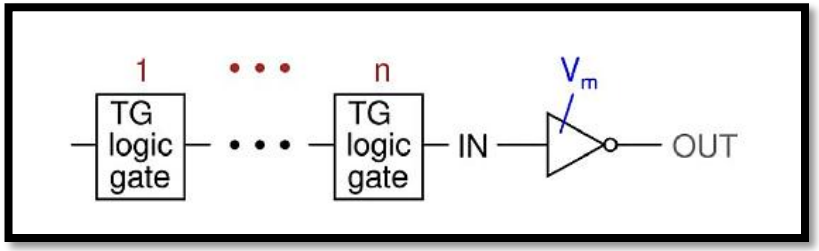
3. After considering the inverter, what other techniques can we apply to other standard cells?
    1. Combinational
    2. Sequential

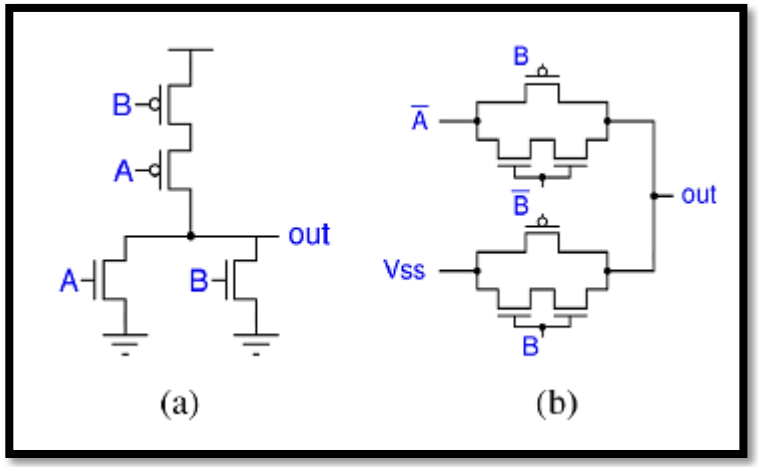
Answers from Week 2

1. Transmission gate based cells for less variation

How to Expand to Logic Gates?

- Problem is weak P/N ratio
- Can be solved with double stack NMOS
- Ratio still high (~6)
  - Ratio technology dependent
- **Solution:** always have both types of transistor
- TX-gate based





Comparison of Methods

	Energy Consumption	Gate Delay	Delay Variation $\left(\frac{\sigma}{\mu}\right)$	$\frac{I_{on}}{I_{off}}$	Area overhead
SubVt technology	✔	?	? (yield)	✔	✘
Min Sized Std Cells	✔	✘	✘	✘	✔
Different Logic Families					
Custom Std. Cell Lib					
Redundancy in Logic Paths	✘		✔	✔	✘
Increase Transistor Length	✔		✔	✔	✔ (Reduce P)
Mixed Vt Inverter	?	?	?	✔	✔
Schmitt trigger inverter	✘	✘	✔	✔	✘
Transmission Gate Logic	✘	?	✔	✔	✔
Low Vt Devices	✘	✔	✘	✘	
NMOS Stacking	✔		✔	✔	✔ (Reduce P)
Transmission Gate Logic	✘	?	✔	✔	✔

References

1. Process Variations, University of Maryland, Advanced VLSI Design:http://www.csee.umbc.edu/~cpatel2/links/640/lectures/lect10_process_var.pdf
2. Reynders, N.; Dehaene, W., "Variation-Resilient Building Blocks for Ultra-Low-Energy Sub-Threshold Design," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.12, pp.898,902, Dec. 2012.